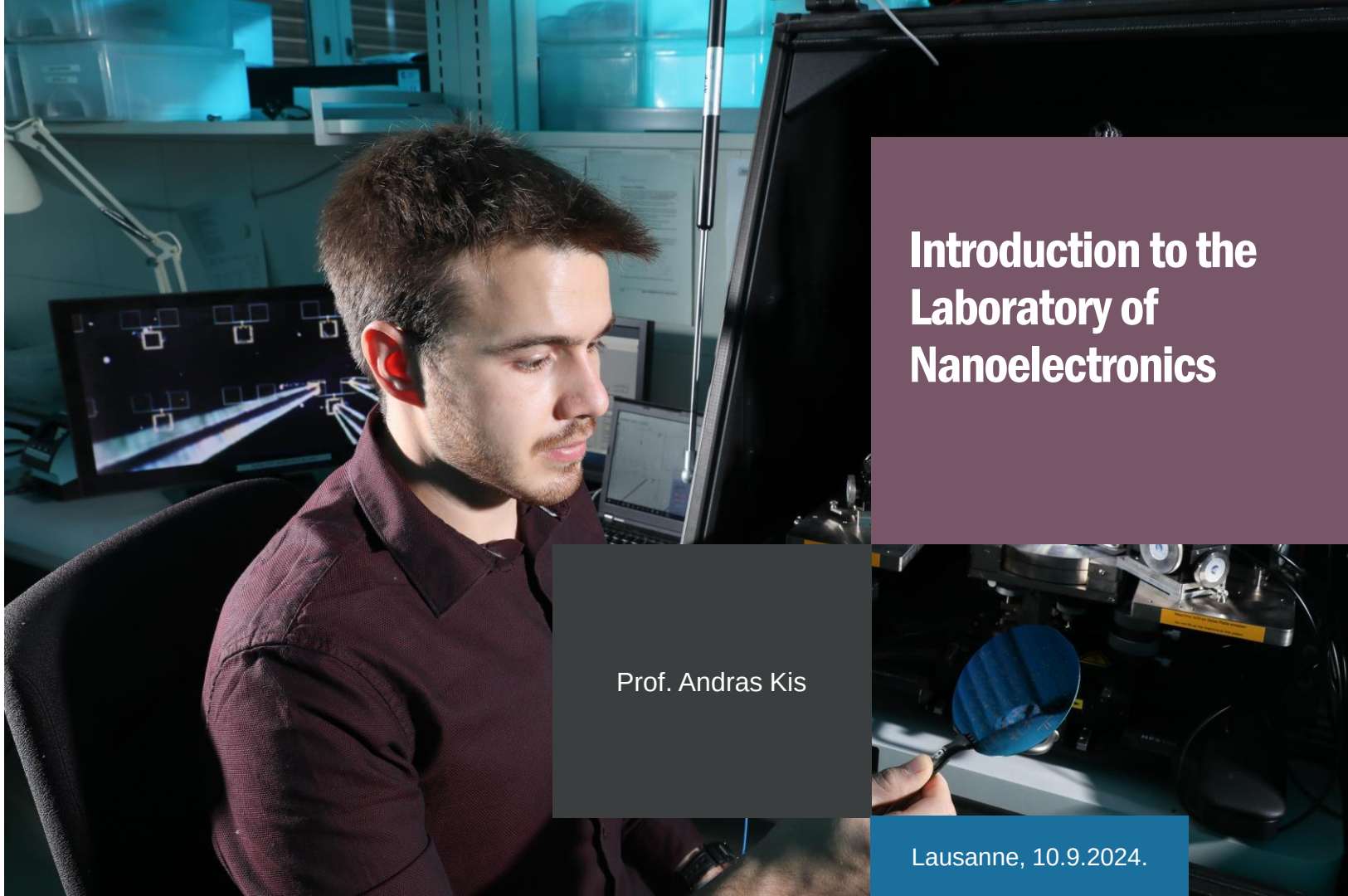
Introduction to the Laboratory of Nanoelectronics



Prof. Andras Kis

Lausanne, 10.9.2024.

Assistants

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Objectives

Learning quantitative approaches in nanoelectronics

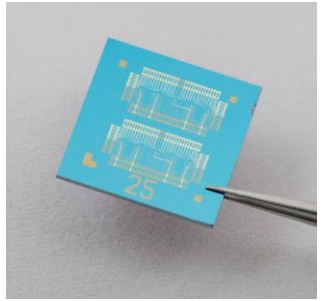
- Learn techniques for fabrication and characterization of functional nanoelectronic devices by going through an actual process flow
- Nanomaterial preparation
- Nanomaterial characterization
- Integration into functional electronic devices
- Characterisation of FETs, memory and optoelectronic devices based on 2D materials

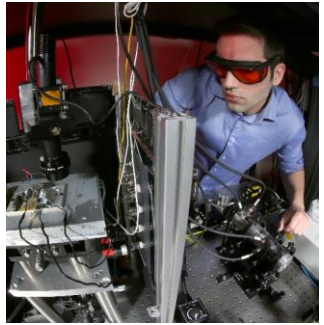
Working in a real-life research lab

- Keeping a professional notebook
- Behavior in a cleanroom
- Planning, organizing and executing a research project
- Writing a scientific paper

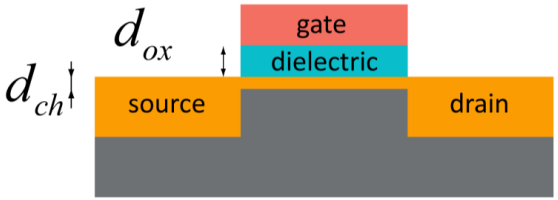
Connected to

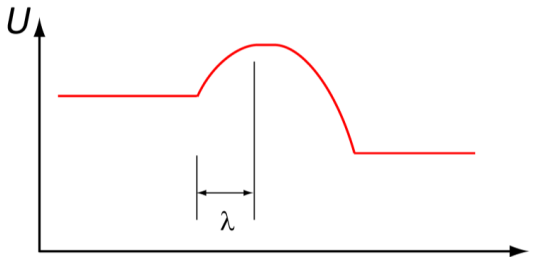
- Semiconductor devices II



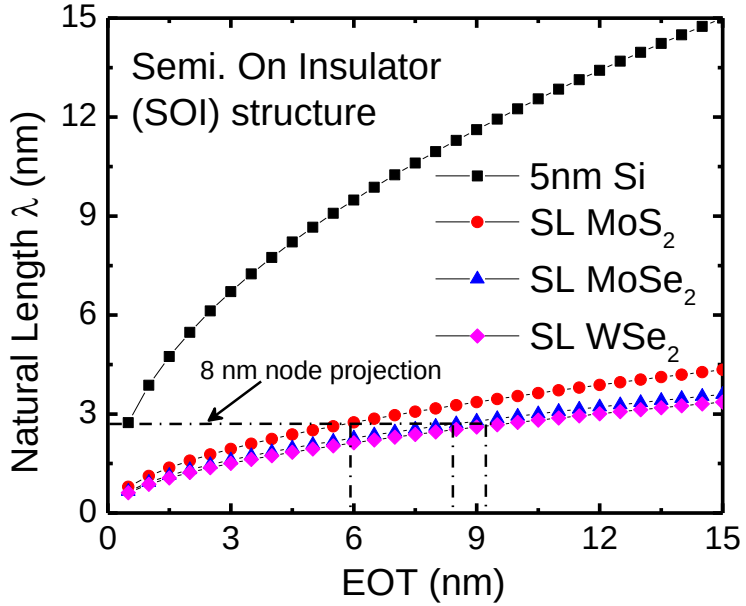


Transistor Scaling





$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} d_{ox} d_{ch}}$$



Material	ε_{ch}	d_{ch} (nm)	λ (nm)	μ (cm^2/Vs)	E_g (eV)
Si SOI	11.9	2	2	10	1.1 indirect
MoS_2	4.3	0.65	0.66	60	1.8 **direct**

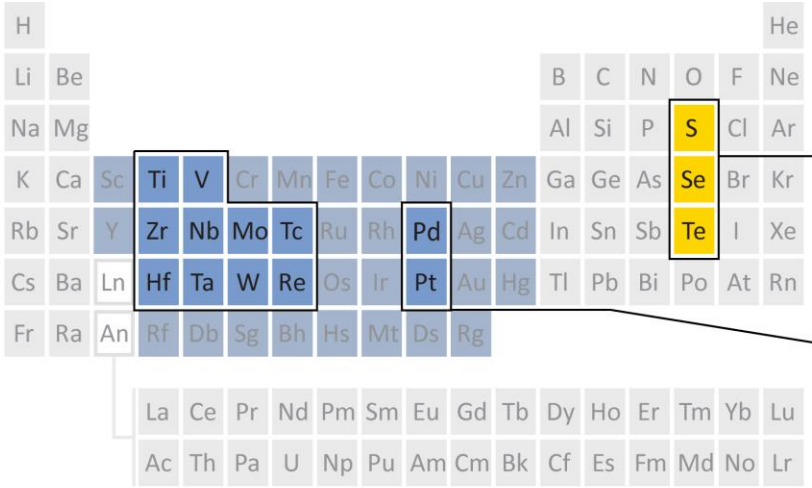
ε_{ox}=3.9, d_{ox} =0.6 nm

Credit: W. Cao and K. Banerjee (UCSB)

Ferain et al., Nature 479, 310 (2011)

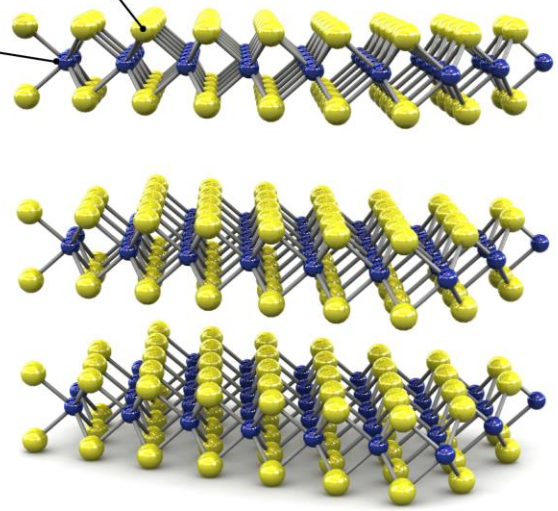
Colinge, Sol. State El. 48, 897 (2004)

2D Transition Metal Dichalcogenides (TMDCs)



Common formula: MX_2

40 stable materials



Semiconductors: MoS_2 $MoSe_2$ WS_2 WSe_2 $MoTe_2$ WTe_2

Semimetals: TiS_2 $TiSe_2$

Metals, CDW, superconductors: $NbSe_2$ NbS_2 $NbTe_2$ TaS_2 $TaSe_2$ $TaTe_2$

IRDS - International Roadmap for Devices and Systems

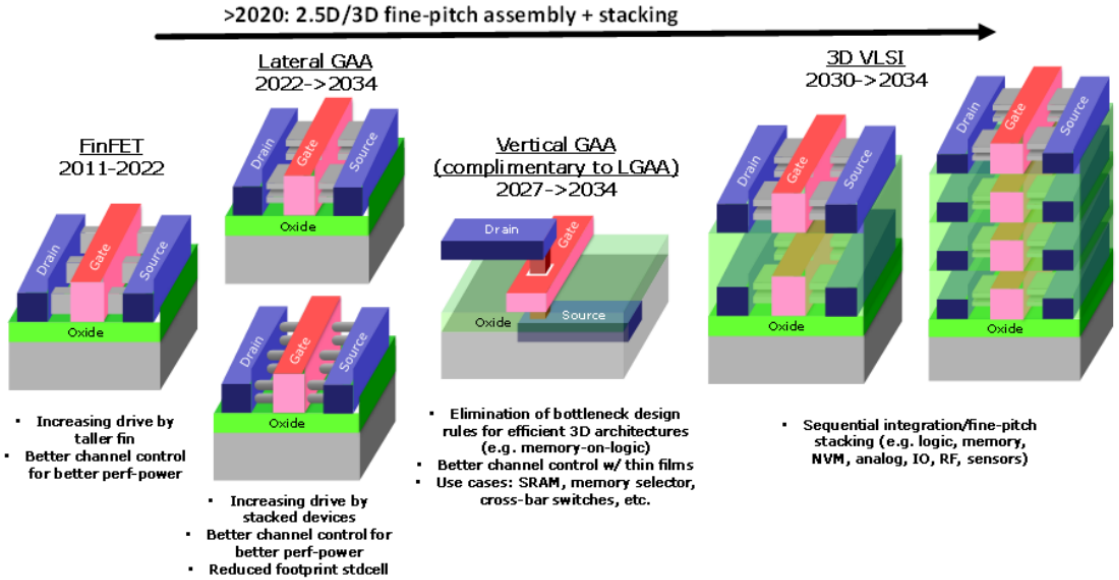


Figure ES48 *Change in the MOSFET device architecture from the 2D planar through 2.5D FinFets to 3D monolithic VLSI with GAA*

https://irds.ieee.org/editions/2021/executive-summary

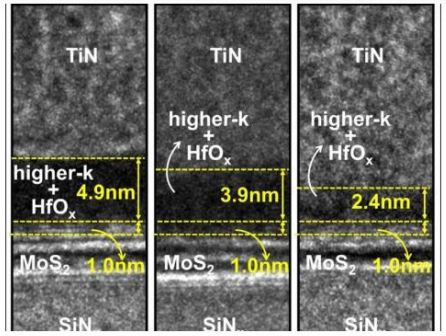
IRDS - International Roadmap for Devices and Systems

YEAR OF PRODUCTION	2021	2022	2025	2028	2031	2034
	G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Platform device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
Frequency scaling - node-to-node	-	0.02	0.16	0.09	-0.08	-0.01
CPU frequency at constant power density (GHz)	3.13	2.83	3.53	2.50	1.48	0.86
Power at iso frequency - node-to-node	-	-0.16	-0.27	-0.05	-0.06	-0.08
Power density - relative	1.00	1.12	1.04	1.59	2.51	4.27
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process technology inflection	Conformal Doping, Contact	Channel, RMG	Lateral/AtomicEtch	Non-Cu Mx	3DVLSI	3DVLSI
Stacking generation inflection	2D	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D-stacking, 3DVLSI: Mem-on-Logic with Interconnect	3D-stacking, 3DVLSI: Logic-on-Logic

Figure ES9 *Devices will continue to aggressively scale in the next 5 years*

https://irds.ieee.org/editions/2021/executive-summary

2D Materials in the Industry



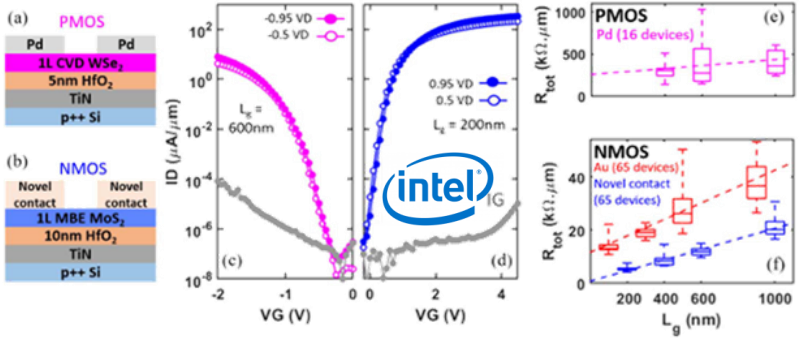
TSMC heads below 1nm with 2D transistors at IEDM

Technology News | October 18, 2022

By Nick Flaherty

MATERIALS & PROCESSES

https://www.eenewseurope.com/en/tsmc-heads-below-1nm-with-2d-transistors-at-iedm/



[INTEL, IEEE TED (2021), doi:10.1109/TED.2021.3118659]

First Demonstration of GAA Monolayer-MoS_2 Nanosheet nFET with 410 μA/μm I_D at 1V V_D at 40nm gate length

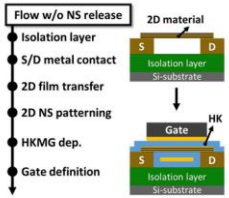


Fig. 19. Process flow and schematic of single 2D NS device without sheet release.

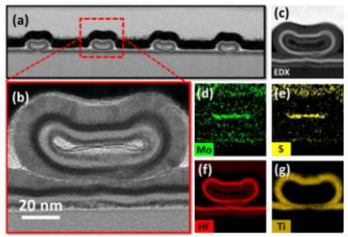


Fig. 20. TEM cross section of (a) and (b) monolayer MoS_2, nanosheet device with gate stack fully wrapped around the channel. Corresponding EDX elemental mapping (d)-(g).

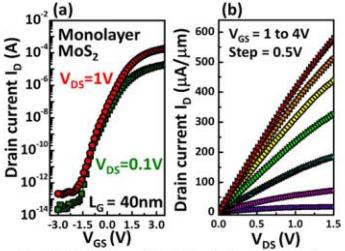


Fig. 21. (a) I_D-V_{GS} and (b) I_D-V_{DS} device characteristics of monolayer MoS_2 NSFET with Lg=40nm.

[TSMC, IEDM (2022), doi:10.1109/IEDM45625.2022.10019563]

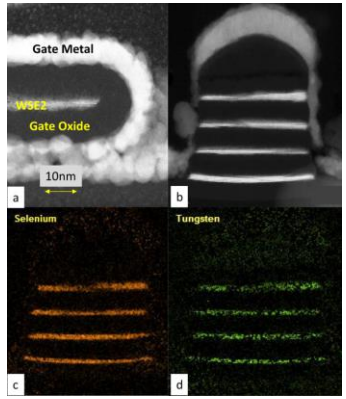
Process integration and future outlook of 2D transistors

https://doi.org/10.1038/s41467-023-41779-5

Kevin P. O'Brien, Carl H. Naylor, Chelsey Dorow, Kirby Maxey, Ashish Verma Penumatcha, Andrey Vyatskikh, Ting Zhong, Ande Kitamura, Sudarat Lee, Carly Rogan, Wouter Mortelmans, Mahmut Sami Kavrik, Rachel Steinhardt, Pratyush Buragohain, Sourav Dutta, Tristan Tronic, Scott Clendenning, Paul Fischer, Ernisse S. Putna, Marko Radosavljevic, Matt Metz & Uygar Avci

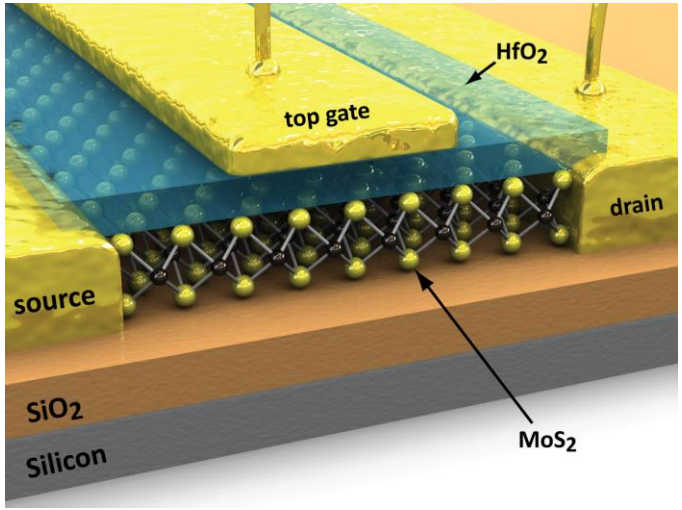
Check for updates

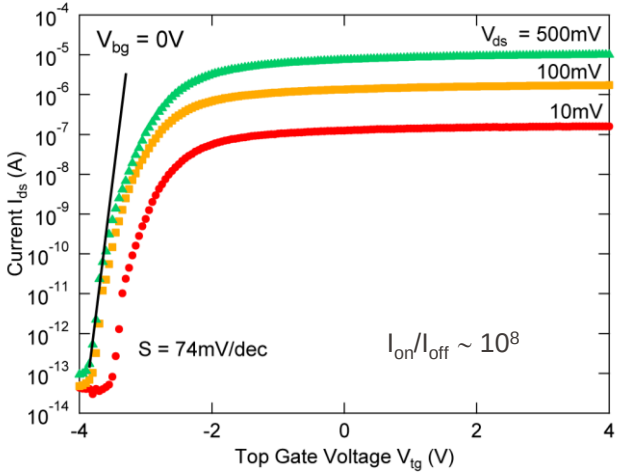
nature communications

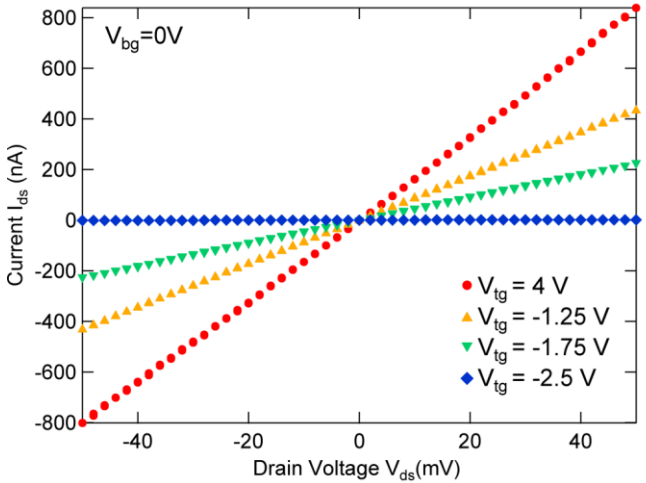


[INTEL, *Nature Comm.* (2023), DOI: 10.1038/s41467-023-41779-5]

2D Transistors and Characterisation

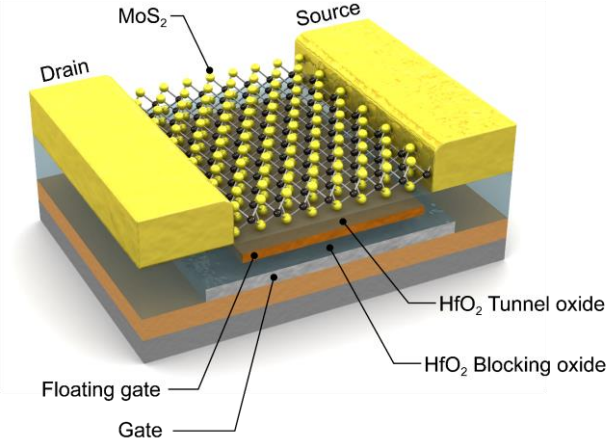


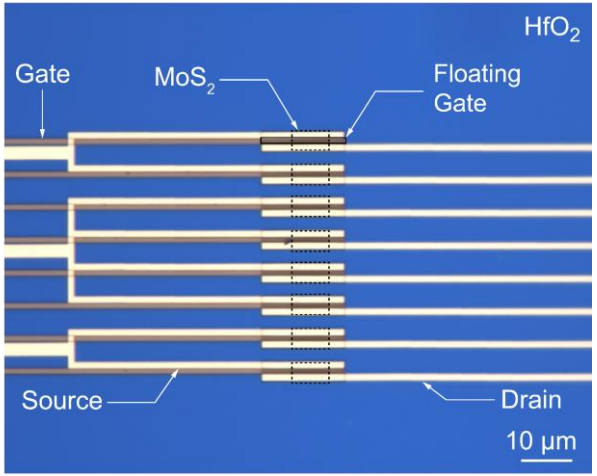


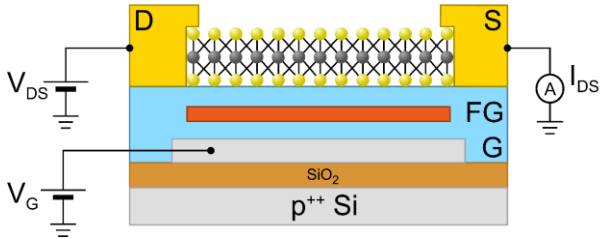


Radosavljevic et al; Nature Nanotechnology 2011

2D Flash Memories and Memristors





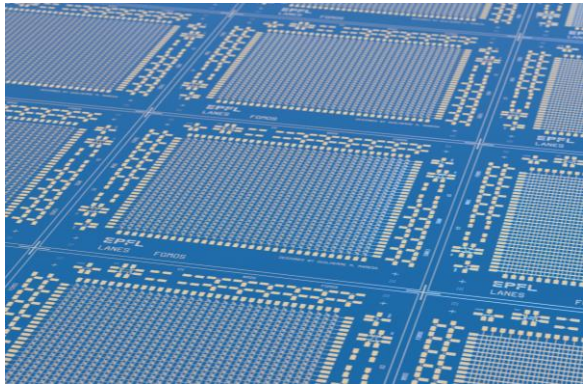


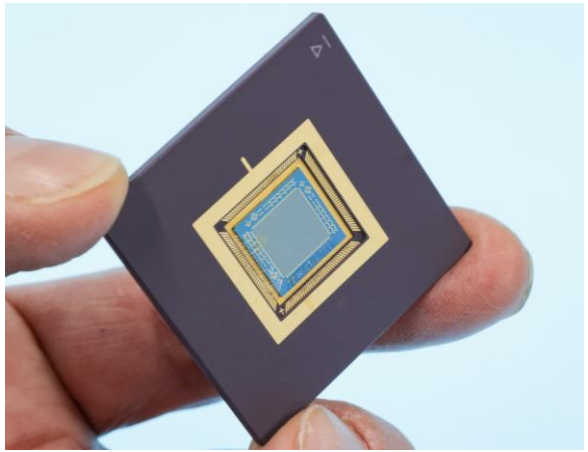
Advantages of 2D for flash memories:

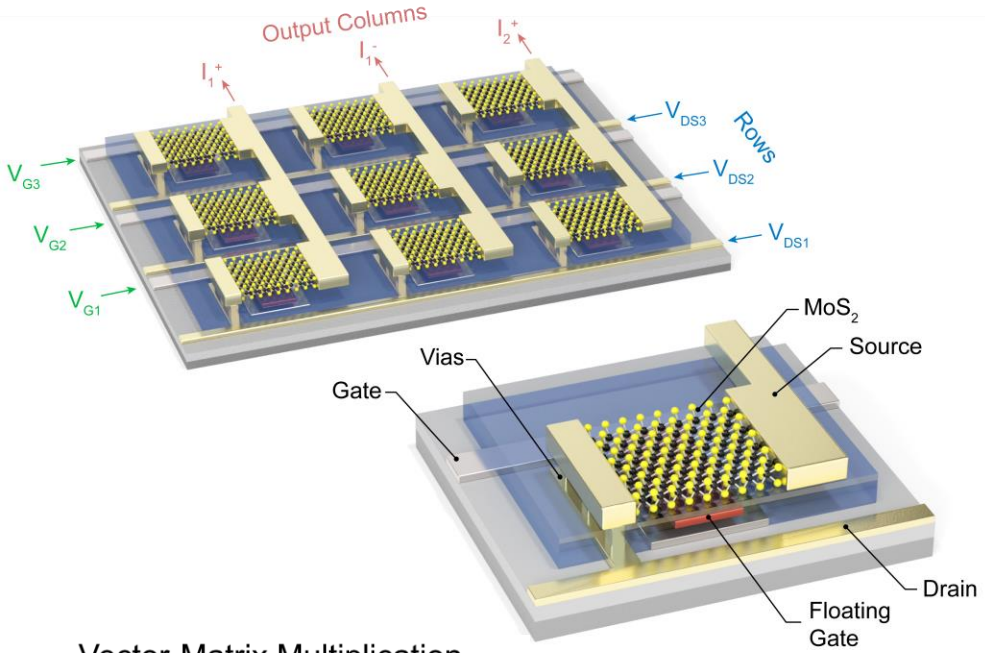
- Reduced cell-to-cell interference
- Multilevel storage
- Possible scaling beyond 12 nm

Migliato Marega et al; Nature 2020

2D Large-scale Integrated circuits







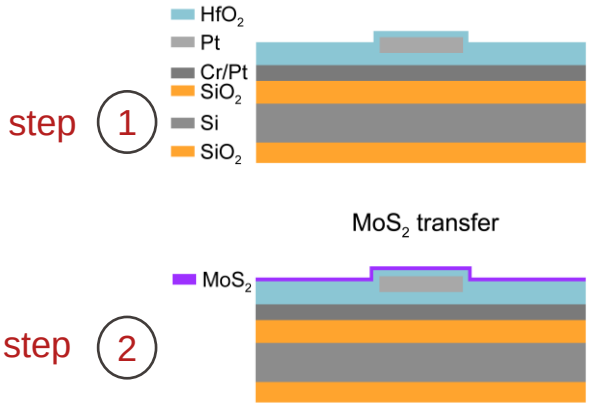
Vector-Matrix Multiplication

$$\begin{bmatrix} I_1^+ \\ I_1^- \\ \vdots \\ I_M^- \end{bmatrix} = \begin{bmatrix} G_{11}^+ & G_{12}^+ & \cdots & G_{1N}^+ \\ G_{21}^- & G_{22}^- & \cdots & G_{2N}^- \\ \vdots & \vdots & \ddots & \vdots \\ G_{M1}^- & G_{M2}^- & \cdots & G_{MN}^- \end{bmatrix} \cdot \begin{bmatrix} V_{DS1} \\ V_{DS2} \\ \vdots \\ V_{DS(N)} \end{bmatrix}$$

Marega…Kis, Nature Electronics, 2023.

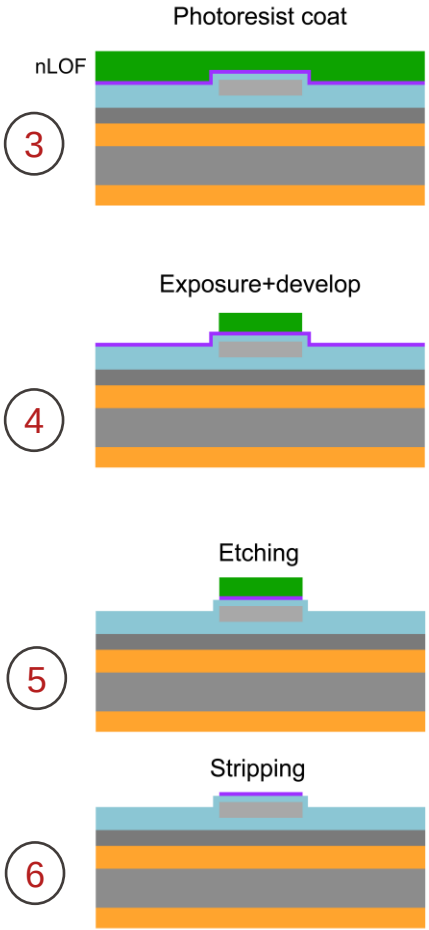
Andras Kis

Process flow

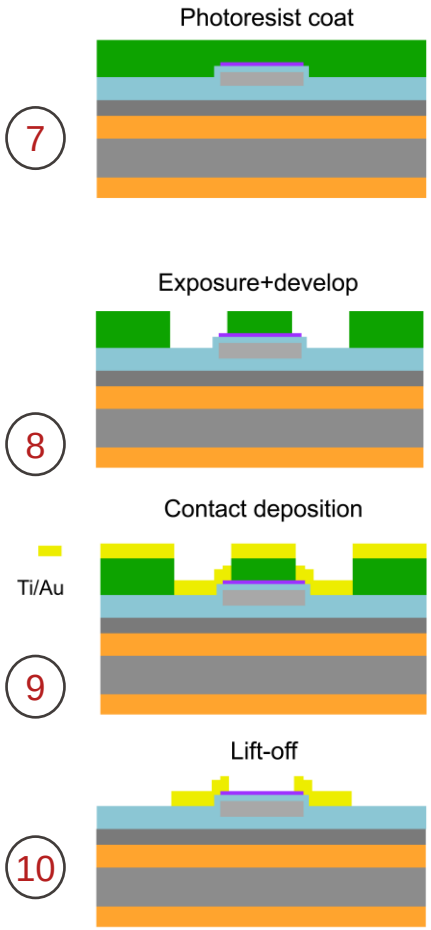


Exercise 1

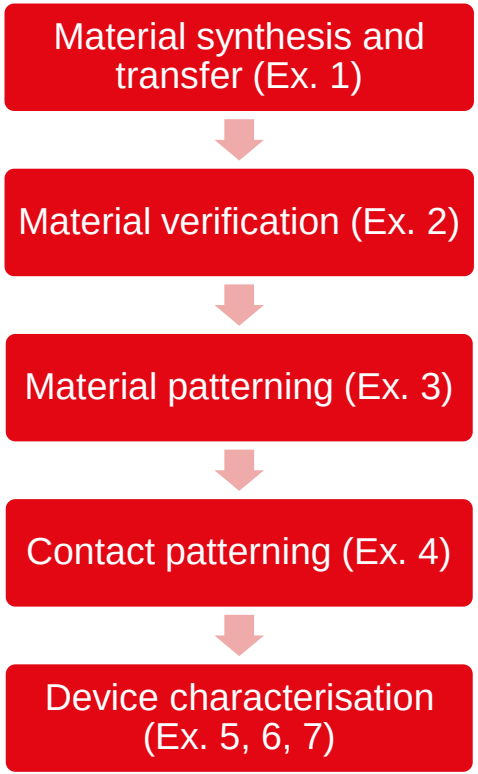
Exercise 3



Exercise 4



Simplified process flow



TP Exercises

Exercise	Location	Assistant
1. MoS_2 transfer	*Omitted in 2024*	*Omitted in 2024*
2. Optical reflectance measurements	MED 2 117 (Photonics TP Lab)	Cristian de Giorgio
3. Laser writer + etching	CMI	Eloi Collette
4. Laser writer + contact evaporation	CMI	Asmund Ottesen
5. Transistor characterisation, TLM	MED 2 1519 (Electronics TP Lab)	Riccardo Chiesa
6. Memory and memristor characterisation	MED 2 1519 (Electronics TP Lab)	Riccardo Chiesa
7. Photodetectors	MED 2 117 (Photonics TP Lab)	Cristian de Giorgio

Organization 2024

Exercise	Location	Meeting point	Assistant
1. MoS_2 transfer	*Omitted in 2024*	*Omitted in 2024*	*Omitted in 2024*
2. Optical reflectance measurements	MED 2 117 (Photonics TP Lab)	MED 2 117	Cristian de Giorgio cristian.degiorgio@epfl.ch
3. Laser writer + etching	CMI	In front of BM building, central entrance, level 1	Eloi Collette eloi.collette@epfl.ch
4. Laser writer + contact evaporation	CMI	In front of BM building, central entrance, level 1	Asmund Ottesen asmund.ottesen@epfl.ch
5. Transistor characterisation, TLM	MED 2 1519 (Electronics TP Lab)	MED 2 1519	Riccardo Chiesa riccardo.chiesa@epfl.ch
6. Memory and memristor characterisation	MED 2 1519 (Electronics TP Lab)	MED 2 1519	Riccardo Chiesa riccardo.chiesa@epfl.ch
7. Photodetectors	MED 2 117 (Photonics TP Lab)	MED 2 117	Cristian de Giorgio cristian.degiorgio@epfl.ch

Course structure

- **Week type 1**: in-laboratory exercises, 4h/week, supervised work in a group, every second week, alternating with:
- **Week type 2**: independent work 4h with available support
  - Complete data analysis
  - Write and submit the report
  - Prepare next exercise
- Exam format: writing a short paper about the results, with support from assistants and the teacher

Calendar

10	SEP, TUE	14:00 – 16:00	TP Nanoelectronics - Intro Session	
17	SEP, TUE	14:00 – 18:00	TP Nanoelectronics - Session 1A	
24	SEP, TUE	14:00 – 18:00	TP Nanoelectronics - Session 1B	
1	OCT, TUE	14:00 – 18:00	TP Nanoelectronics - Session 2A	
8	OCT, TUE	14:00 – 18:00	TP Nanoelectronics - Session 2B	
15	OCT, TUE	14:00 – 18:00	TP Nanoelectronics - Session 3A	
22	OCT, TUE	14:00 – 18:00	FALL BREAK	
29	OCT, TUE	14:00 – 18:00	TP Nanoelectronics - Session 3B	
5	NOV, TUE	14:00 – 18:00	TP Nanoelectronics - Session 4A	
12	NOV, TUE	14:00 – 18:00	TP Nanoelectronics - Session 4B	
19	NOV, TUE	14:00 – 18:00	TP Nanoelectronics - Session 5A	
26	NOV, TUE	14:00 – 18:00	TP Nanoelectronics - Session 5B	
3	DEC, TUE	14:00 – 18:00	TP Nanoelectronics - Session 6A	
10	DEC, TUE	14:00 – 18:00	TP Nanoelectronics - Session 6B	
17	DEC, TUE	14:00 – 18:00	TP Nanoelectronics - Catch-up	

Teaching material

- Handouts and instructions for the respective exercise
- Reference materials from the exercises
- Lectures and recordings for the course “Semiconductor devices II”

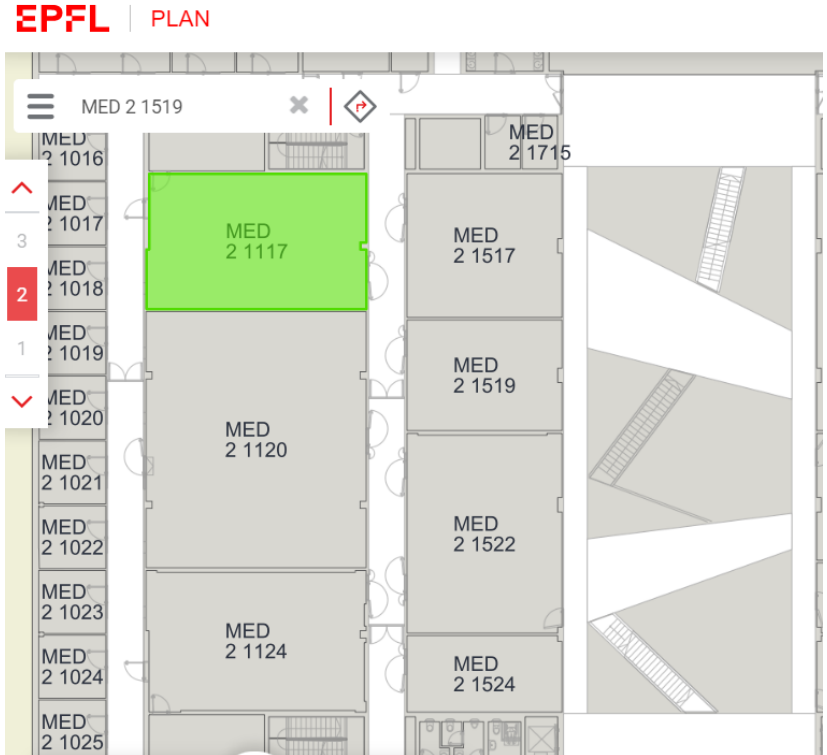
Evaluation

What	Grade	Outcome
Quiz by TA, assessing preparation for the exercise	Pass/fail	If fail, cannot proceed with the exercise
Report	1-6, 60% weight in the final grade	1 if failed the preparation or no-show*
Exam in the written form, final paper	1-6, 40% of the grade	

*One “rattrapage” session possible

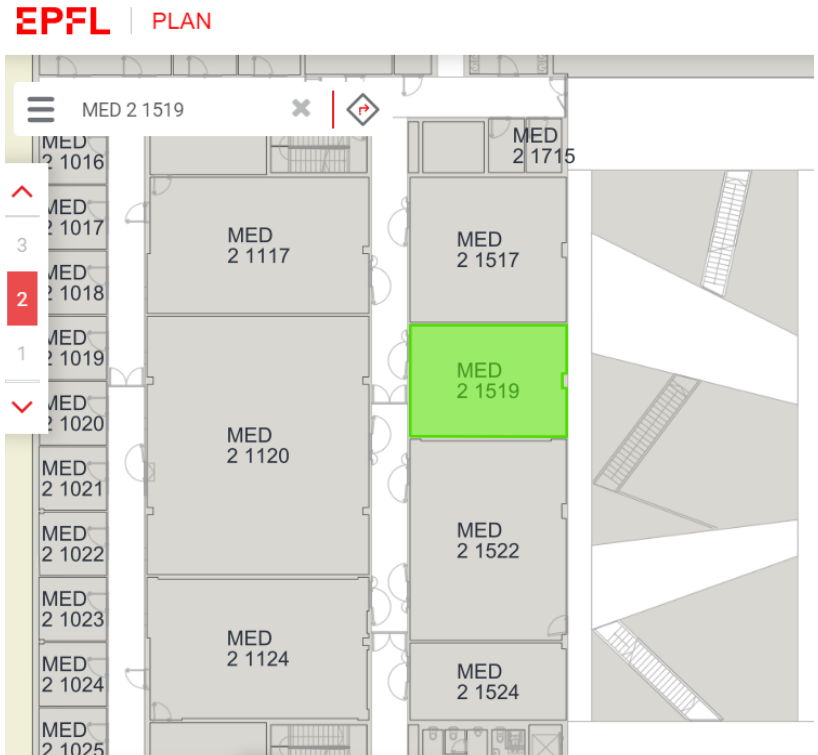
Locations

- MED 2 1117 (Ex 2,7)
  https://plan.epfl.ch/?room==MED%202%201117
- Meeting point: the actual room



Locations

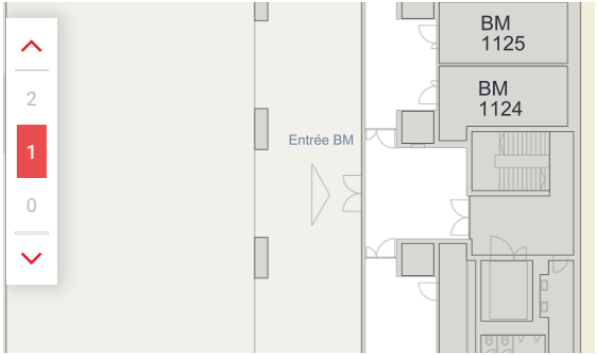
- MED 2 1519 (Ex 5,6)
  https://plan.epfl.ch/?room==MED%202%201519
- Meeting point: the actual room



Locations

- CMI (Ex. 3, 4)

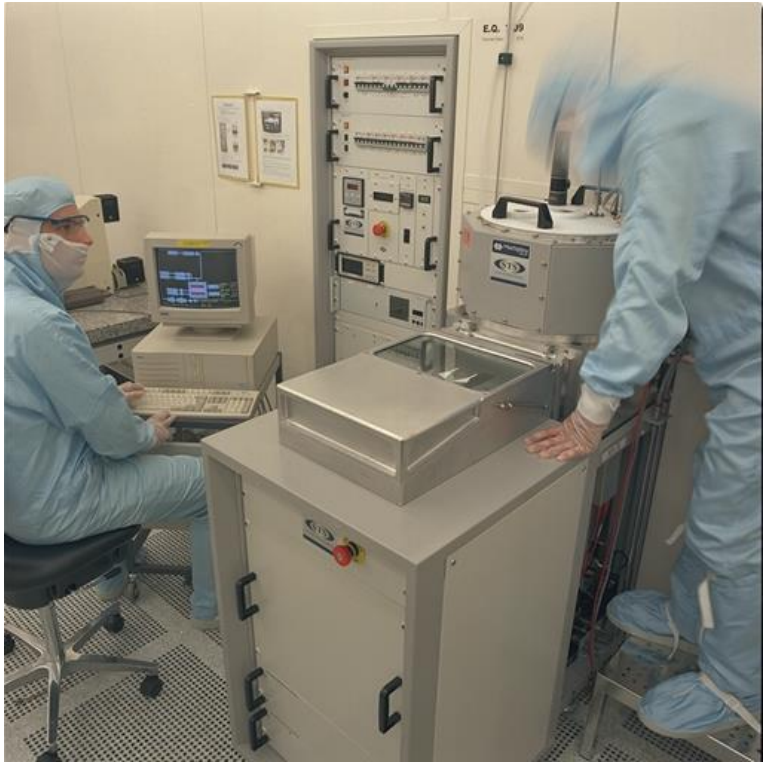
- **Meeting point:** central entry to the BM building



Cleanroom safety and general rules

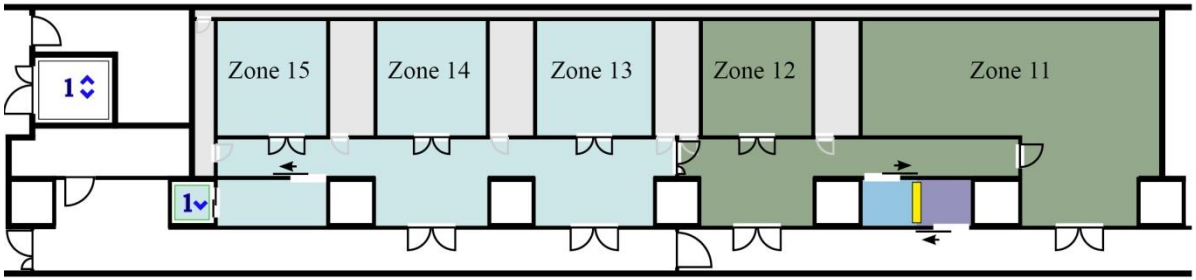
CMi EPFL Center of MicroNanoTechnology

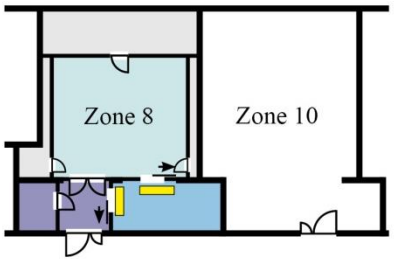
Cleanroom description

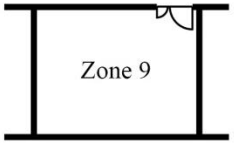


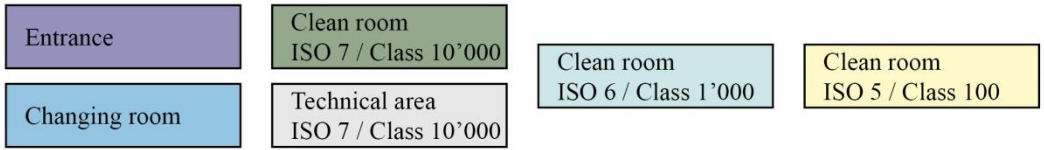
Cleanroom description

CMI
BM+1

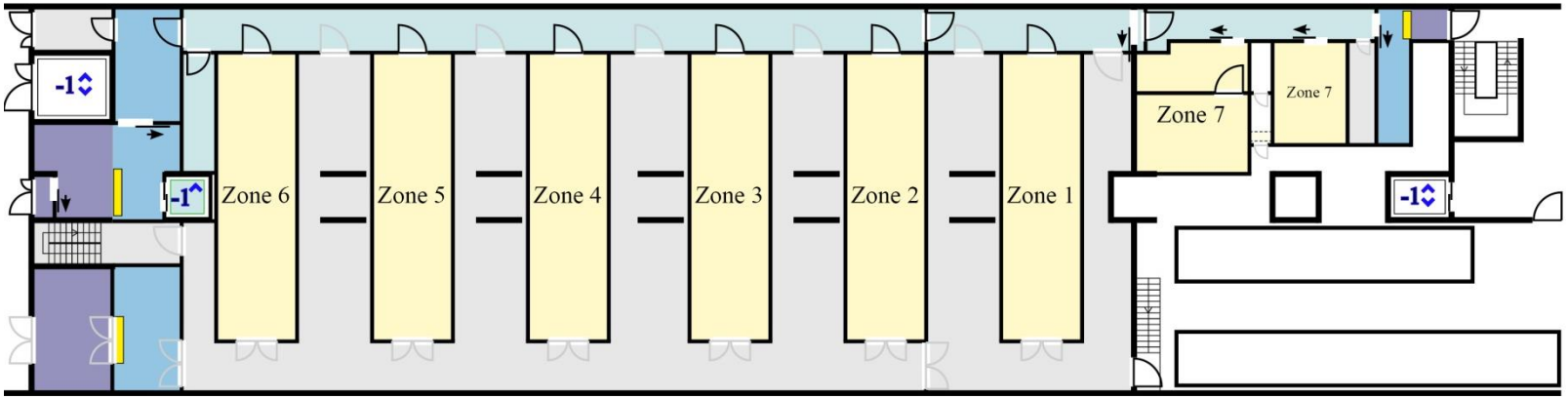






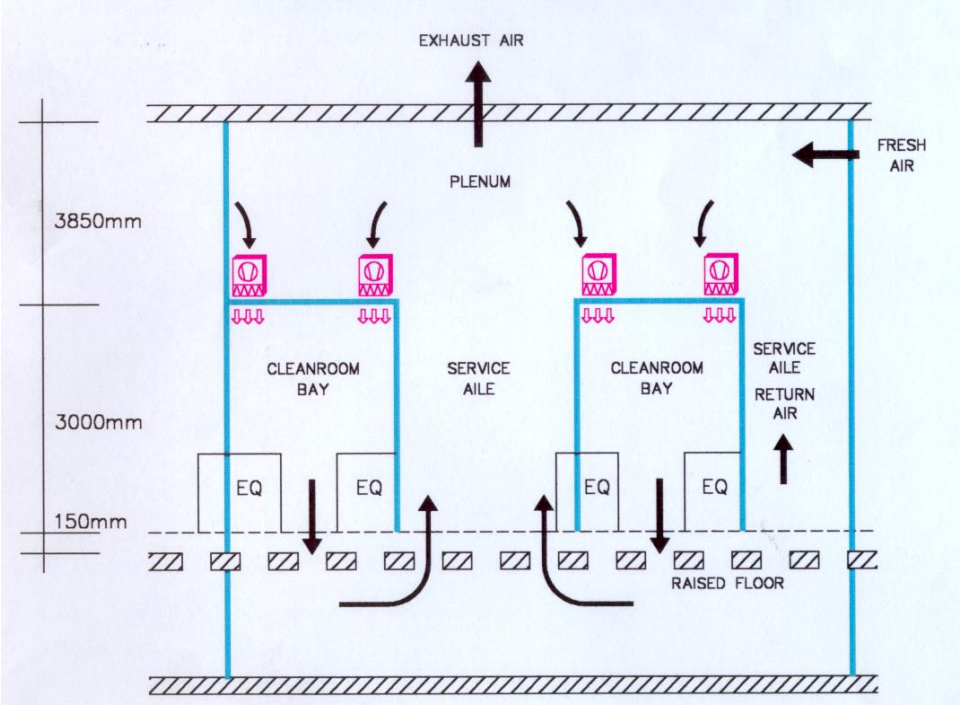


CMI
BM-1



Cleanroom description

- Air filtration and circulation



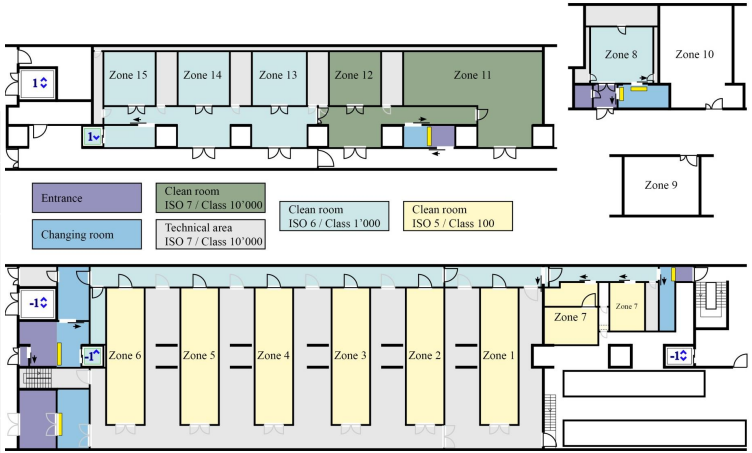
ACTUAL VALUES :
(2/3 of maximum capacity)

- **FRESH AIR**
  - 38’000 m^3/h
  - filter efficiency : 99.97% for particles size 0.1-0.3 µm
- **EXHAUST**
  - 36 ’000 m^3/h
- **FFU**
  - 167 units
  - 0.7 m^2 active area
  - total: 189’000 m^3/h
  - filter efficiency : 99.999% for particles size 0.1-0.3 µm

Cleanroom description

Airborne Particulate Cleanliness Classes (by cubic meter):

CLASS	Number of Particles per Cubic Meter by Micrometer Size					
	0.1 micron	0.2 micron	0.3 micron	0.5 micron	1 micron	5 microns
ISO1	10	2				
ISO2	100	24	10	4		
ISO3	1,000	237	102	35	8	
ISO4	10,000	2,370	1,020	352	83	
ISO5	100,000	23,700	10,200	3,520	832	29
ISO6	1,000,000	237,000	102,000	35,200	8,320	293
ISO7				352,000	83,200	2,930
ISO8				3,520,000	832,000	29,300
ISO9				35,200,000	8,320,000	293,000



Source: https://www.terrauniversal.com/blog/fs209e-and-iso-cleanroom-standards/

Dressing CMI BM-1

- Overshoes
- Cleanroom suit

Dressing CMI BM-1

- Overshoes
- Cleanroom suit
- Cleanroom boots
- Face mask
- Vinyl gloves
- Safety googles
- CAMIPRO card

General behavior in the cleanroom

- Never work alone in a zone
- No more than 6 people in a zone
- Walk normally, do not run
- Do not shake hands
- Do not work in the cleanroom if you have a cold
- In case of evacuation alarm, follow the safety rules
- Only staff fix the machines

General cleanroom rules

- Lint-free cleanroom paper only
- Cleanroom notebooks available through CMi ordering system
- Pens are available in each zone
- Photocopier can be used to transfer notes in and out of the cleanroom
- PC access to public folders in each zone

Prohibited:
Regular paper
Graphite pencils & regular pens

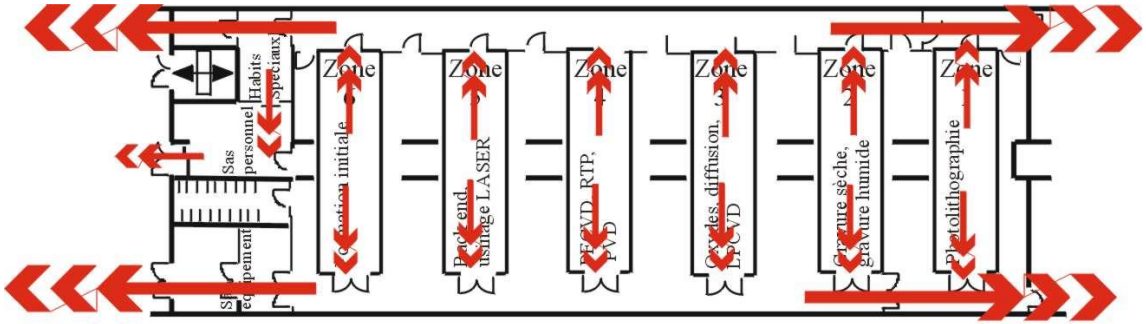
Cleanroom safety rules

- Never Work Alone
- Only One Emergency N° : 115
- Report any safety problems you encounter
- Wear protective glasses or Medical glasses all the time

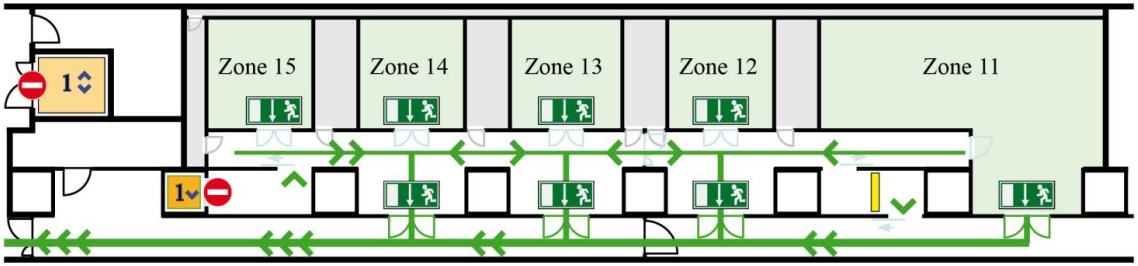
prohibited:
normal paper
Graphite pencils & normal pens

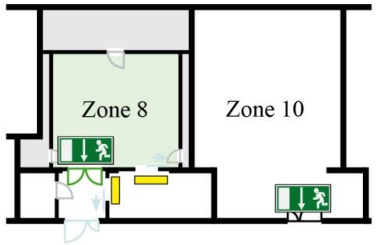
Alarms and evacuation

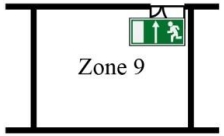
- Double Tone Horn
- Flashing **Red** Light
- ⇒ **Evacuate immediately with cleanroom dressing**
- **Meeting point: BM 1.125 (Ph. Flückiger office) wait there to be accounted for**
- remark : red alarm can be activated by the push-buttons



Alarms and evacuation







convention is that